Claims

What is claimed is:

1. A method for implementing power control in multi-voltage input/output (I/O) circuits comprising the steps of:

providing first current biasing devices for creating a first constant bias current;

providing second current biasing devices for creating a second bias current; and

activating said second current biasing devices at a first voltage; and deactivating said second current biasing devices at a second voltage; said first voltage being less than said second voltage.

2. A method for implementing power control as recited in claim 1 wherein the step of providing said first current biasing devices for creating said first constant bias current includes the steps of constantly activating said first current biasing devices at both said first voltage and said second voltage.

3. A method for implementing power control as recited in claim 1 wherein the step of providing said second current biasing devices for creating said second bias current includes the steps of providing said second current biasing devices in parallel with said first current biasing devices; and applying a control input to said second current biasing devices for selectively activating said second current biasing devices at said first voltage; and deactivating said second current biasing devices at said second voltage.

4. A method for implementing power control as recited in claim 1 wherein each of the steps of providing said first current biasing devices and providing said second current biasing devices includes the steps of providing a plurality of field effect transistors (FETs).

5. A method for implementing power control as recited in claim 4 includes the steps of providing respective field effect transistors (FETs) of said second current biasing devices in parallel with respective field effect transistors (FETs) of said first current biasing devices.

6. A method for implementing power control as recited in claim 5 includes the steps of connecting a gate input of respective field effect transistors (FETs) of said first current biasing devices to a gate input of respective field effect transistors (FETs) of said second current biasing devices at said first voltage and disconnecting said gate inputs of respective field effect transistors (FETs) of said second current biasing devices at said second voltage.

7. A method for implementing power control as recited in claim 1 wherein the steps of activating said second current biasing devices at a first voltage; and deactivating said second current biasing devices at a second voltage includes the steps of providing a bias control generating circuit coupled to said second current biasing devices for activating said second current biasing devices at said first voltage; and deactivating said second current biasing devices at said second voltage.

8. A method for implementing power control as recited in claim 1 wherein the steps of activating said second current biasing devices at a first voltage; and deactivating said second current biasing devices at a second voltage includes the steps of providing a bias control generating circuit for generating a control input for activating said second current biasing devices at said first voltage; and generating said control input for deactivating said second current biasing devices at said second voltage.

9. A method for implementing power control as recited in claim 8 wherein said control input includes a gate input applied to respective field effect transistors (FETs) of said second current biasing devices.

10. Apparatus for implementing power control in multi-voltage input/output (I/O) circuits comprising:

a first set of current biasing devices for creating a first constant bias current;

a second set of current biasing devices for creating a second bias current; and

a control input for activating said second set of current biasing devices at a first voltage; and for deactivating said second set of current biasing devices at a second voltage; said first voltage being less than said second voltage.

11. Apparatus for implementing power control as recited in claim 10 includes a bias control generating circuit for generating said control input.

12. Apparatus for implementing power control as recited in claim 10 wherein each of said first set of said current biasing devices and said second set of said current biasing devices includes a plurality of field effect transistors (FETs).

13. Apparatus for implementing power control as recited in claim 12 wherein said plurality of field effect transistors (FETs) of said first set of said current biasing devices are constantly activated and controlled by a constant gate input.

14. Apparatus for implementing power control as recited in claim 12 wherein said plurality of field effect transistors (FETs) of said second set of said current biasing devices are selectively activated at said first voltage and controlled by a switched gate input.

15. Apparatus for implementing power control as recited in claim 14 wherein said plurality of field effect transistors (FETs) of said second set of said current biasing devices are coupled to a bias control generating circuit providing said switched gate input and selectively activated at said first voltage.